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EXECUTIVE SUMMARY

The deliverable (D5.1) comprises a comprehensive presentation of the developed control techniques, showcasing the functionality and expected performance benefits of the solutions on simulation level.

The first part of the deliverable addresses advanced sensing and control methods for improved converter performance. High-bandwidth sensing is treated as an enabling layer for advanced control, fast protection, device monitoring, and diagnostic functions. The second part focuses on computational control for reliability. The reported developments provide modelling, sensing, and control-oriented foundations for reducing thermal stress, degradation diagnostics, and improving reliability-oriented operation. The third part addresses self-learning and data-driven control for resilience.

Overall, this preliminary report consolidates the progress on sensing, modelling, control, and data-driven decision-making for advanced power electronic systems. The results reported at this stage include requirements, modelling frameworks, and simulation-based assessments that form the basis for further development, integration, and validation in the project demonstrators.

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1 Introduction

This deliverable presents the preliminary outcomes of Work Package 5, which focuses on advanced power electronics control strategies. The work package addresses sensing hardware and algorithms, control algorithm design, control hardware, and controller implementation for wide-bandgap-based converter and drive systems. The reported developments are intended to support the project use-case demonstrators.

The overall objective of WP5 is to develop data-informed and computational control systems with self-learning capabilities to improve converter performance, extend equipment lifetime, and enhance system availability. In line with this objective, the deliverable is structured around three main technical directions: advanced computational control for superior performance, computational control for reliability, and self-learning data-driven control for resilience.

The first part of the deliverable addresses advanced sensing and control methods for improved converter performance. High-bandwidth sensing is treated as an enabling layer for advanced control, fast protection, device monitoring, and diagnostic functions. Building on sensing capabilities, the deliverable then reports advanced control and modulation concepts for high-switching-frequency WBG-based converters. The second part focuses on computational control for reliability. The reported work combines sensor-based monitoring, digital-twin, modulation-based degradation detection and data-driven condition monitoring systems. The reported developments provide modelling, sensing, and control-oriented foundations for reducing thermal stress, degradation diagnostics, and improving reliability-oriented operation. The third part addresses self-learning and data-driven control for resilience. A machine-learning-enhanced control architecture for a WBG T-Type inverter driving an in-wheel permanent magnet synchronous motor has been presented.

Overall, this preliminary report consolidates the progress in WP5 on sensing, modelling, control, and data-driven decision-making for advanced power electronic systems. The results reported at this stage include requirements, modelling frameworks, and simulation-based assessments that form the basis for further development, integration, and validation in the project demonstrators.

2 Advanced Power Electronics Control Strategies

2.1 Advanced Computational Control for Superior Performance

This section covers the simulation-based developments carried out within Task 5.1 of Work Package 5, including two Subtasks: 5.1.1, which focuses on advanced high-bandwidth sensing, and 5.1.2, which focuses on advanced control for WBG-based converters with high switching frequency.

2.1.1 Advanced High-Bandwidth Sensing

This section covers the conceptual development of advanced high-bandwidth sensing at the simulation level. The work focused on defining the system architecture, specifying technical requirements, and assessing the integration capabilities of the proposed solutions. First, the specifications of a dual-path sensing and protection architecture for a 400 V T-type inverter are presented. This is followed by the sensor requirements and data acquisition architecture for high-bandwidth voltage and current sensing.

The section then introduces the specifications and design of an FPGA-based, low-latency measurement and control architecture. Finally, it presents the high-bandwidth sensing and burst-mode ADC specifications developed for adaptive smart gate driver ICs.

2.1.1.1 Specification of a Dual-Path Sensing and Protection Architecture for a 400 V T-Type Inverter (UC2b)

The measurement and sensing architecture for the 400 V T-Type inverter is defined around two measurement paths with different functions: a microcontroller-based path for control and monitoring, and a gate-driver-based path for local protection and device monitoring. The second path uses the integrated sensing and protection functions of the gate driver to enable local overvoltage, junction-temperature, and short-circuit-related protection functions through gate-driver-integrated ADC, comparator, and DESAT functions.

The microcontroller-based sensing path is specified around an AURIX™ microcontroller with delta-sigma ADCs and time-multiplexed SAR ADC resources. This path covers phase current measurement, rotor position feedback, DC-link voltage measurement, and neutral-point voltage measurement. The ADC configuration supports high-bandwidth signal acquisition, including fast current dynamics required for advanced control strategies.

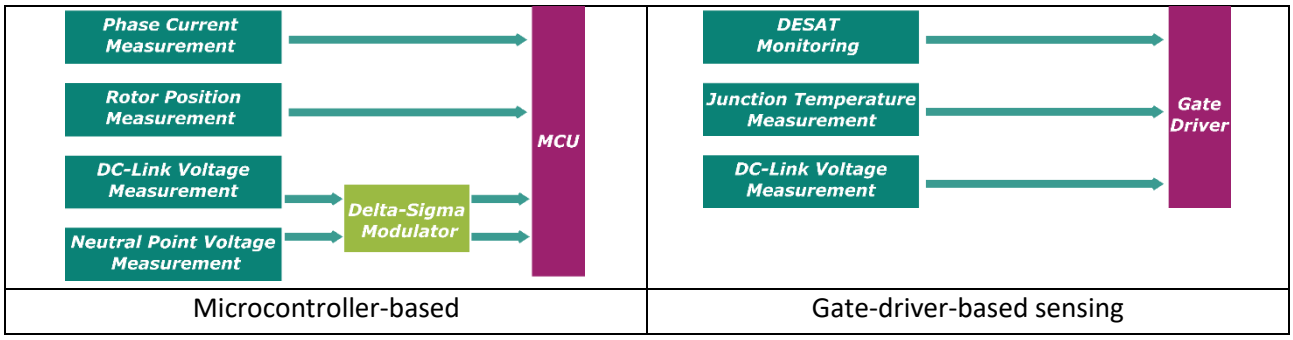


Figure 2-1: Block diagram representation of measurement and sensing architecture

Phase current sensing is specified using dedicated current sensors positioned in each phase leg and connected to the microcontroller through the delta-sigma ADC (DSADC) Digital Communication Interface. Rotor position feedback is defined through two possible sensing configurations: resolver-based angular position detection or encoder-based sensing with selectable quadrature or sine/cosine signal processing.

For the T-Type inverter topology, DC-link and neutral-point voltage measurements are included to support neutral-point balancing and device protection. The voltages V_{DC+}, V_{DC-}, and the neutral-point voltage are

scaled using resistive voltage dividers and processed through external sigma-delta modulation before being filtered and used by the control system.

The gate-driver-based sensing path is specified for device-level protection and monitoring. The smart gate driver integrates ADC and comparator functions that enable local protection decisions without relying on the microcontroller. Because these protection decisions are handled locally in the gate driver, short-circuit and overvoltage events can be acted on without waiting for microcontroller-level processing.

The defined gate-driver protection functions include DC-link overvoltage monitoring through a comparator-based hardware path, junction temperature acquisition through the internal ADC, and short-circuit protection using desaturation monitoring. In the event of a detected short circuit, the DESAT function is intended to trigger fault flags and initiate protective actions through the gate-driver logic. Active Miller clamping is included as an additional gate-level protection function during fault conditions.

System-level communication is defined through an SPI interface between the microcontroller and the gate driver for configuration, status exchange, and fault reporting. Additional external communication and data-acquisition interfaces are planned through CAN and data acquisition systems (DAS), with access through the OneEye™ graphical user interface for system control and monitoring.

2.1.1.2 Preliminary Requirements and Data Acquisition Architecture for High-Bandwidth Voltage and Current Sensing (UC4b)

A preliminary specification has been defined for high-bandwidth voltage and current sensing in the UC4b demonstrator. The objective is to provide isolated, embedded, and programmable measurement capability for GaN- and SiC-based converter systems, providing measured voltage and current data for converter control, diagnostic evaluation, event capture, and visualization.

The preliminary sensor requirements cover four main measurement categories: DC-link voltage, DC-link current, and phase or device-current-related measurements. The voltage channels are specified for wide voltage ranges, galvanic isolation, and sampling rates in the range of approximately 100–200 kS/s. The current channels require higher bandwidth and lower latency, with sampling rates up to 1–2 MS/s for phase-current or device-current-related measurements. The specified sampling ranges distinguish between voltage channels and current channels for fast transient and short-circuit-relevant information.

Based on these requirements, a mixed data acquisition architecture is proposed. Instead of using a single ADC concept for all channels, the architecture distinguishes between medium-speed voltage channels and high-speed current channels. Medium-speed voltage measurements can be handled using multi-channel simultaneous-sampling DAS, while fast voltage and current measurements require low-latency simultaneous-sampling successive approximation register (SAR) ADCs with higher sampling capability.

The proposed architecture includes dedicated ADCs, isolated front-end signal conditioning where required, and a deterministic digital capture stage. An FPGA or dedicated high-speed microcontroller is proposed as a data aggregator to acquire multiple high-speed ADC streams in parallel, avoid SPI serialization bottlenecks, align simultaneous-sampling channels, timestamp data, and perform optional pre-processing. Such pre-processing may include filtering, offset compensation, threshold detection, event capture, packet framing, and data reduction.

Only the required information is intended to be transferred to the host processor or visualization and control system. Depending on the operating mode, this may include raw burst data, decimated measurement streams, calculated RMS or phase information, fault flags, and event windows. This approach reduces processor load and supports integration with higher-level control, diagnostic, and visualization functions.

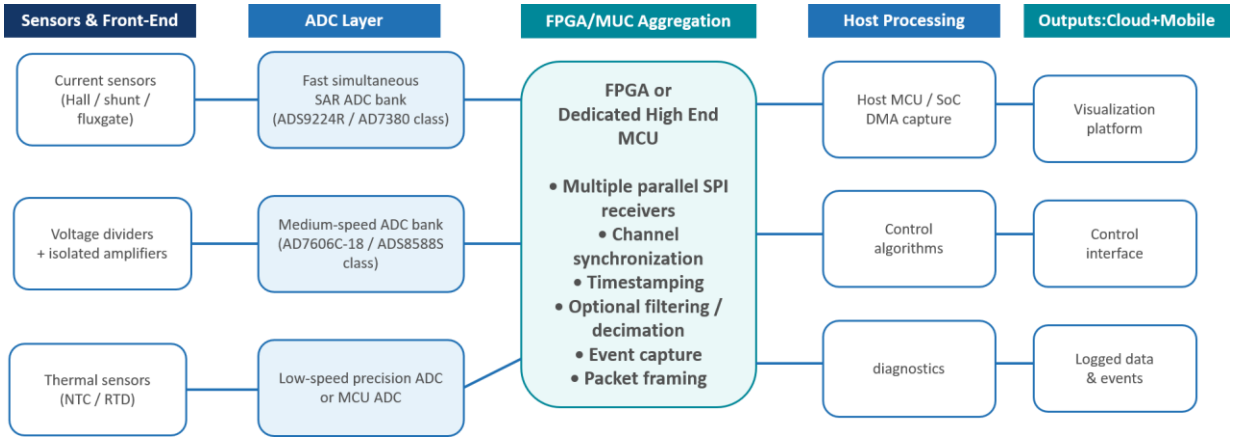


Figure 2-2: Preliminary System Architecture

2.1.1.3 FPGA-Based Low-Latency Measurement and Control Architecture (UC4b)

An FPGA-based measurement and control architecture has been defined for synchronous acquisition of high-bandwidth current and fast response to grid disturbances. The architecture is based on a Xilinx Zynq SoC platform, which combines programmable logic and an embedded processor in a single device. The programmable logic is used for latency-sensitive real-time functions, while the processor is used for higher-level monitoring, data handling, and communication tasks.

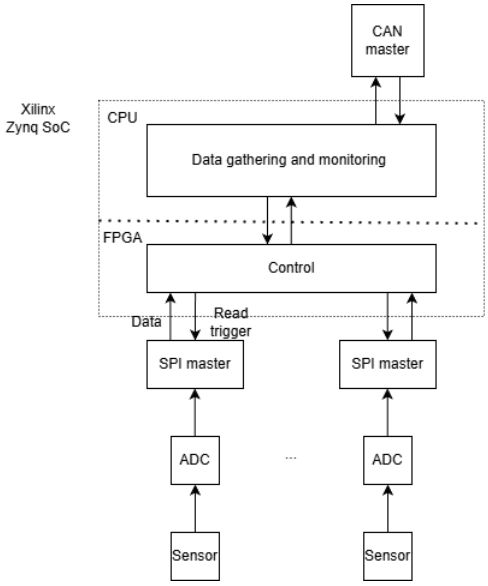


Figure 2-3: Simplified architecture of the measurement and control system on the Xilinx Zynq SoC platform

The main objective of the architecture is to reduce latency between measurement acquisition and control actuation. For this purpose, current and voltage sensor data acquisition and control execution are placed directly in the FPGA fabric. This avoids software communication overhead between separate sensing and control layers and enables deterministic timing for parallel measurement processing.

The FPGA section contains parallel SPI master modules for acquiring data from multiple external ADCs, as well as the main control logic. The control logic generates synchronized read triggers for all SPI masters, receives the measured sensor values, and executes the control algorithms. Measurement and status data generated in the FPGA are transferred to the processor via shared RAM, where they can be collected and

prepared for transmission via CAN. This provides access to internal system variables for monitoring, debugging, and validation during development.

The current system configuration includes four high-priority current sensors that require fast and synchronous sampling, together with eight additional sensors for voltage and Hall-effect measurements. Each sensor is connected through an external ADC via SPI. To avoid the timing limitations of conventional microcontroller-based SPI acquisition, multiple SPI master modules are instantiated in parallel in the FPGA. After a trigger from the control logic, all SPI masters start the conversion and readout process simultaneously, execute their state machines independently, store the acquired data in output registers, and assert a data-ready signal for the controller.

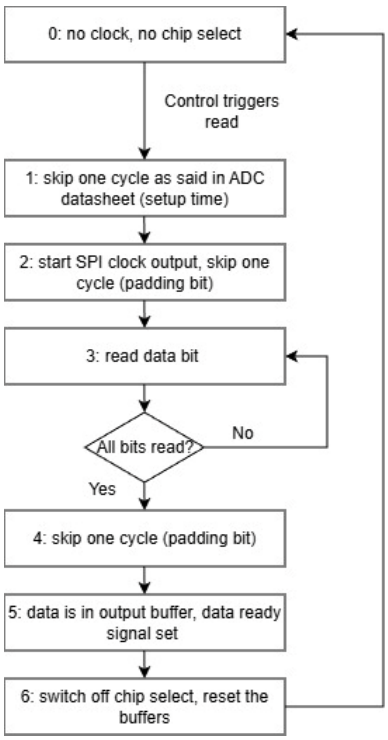


Figure 2-4: SPI master state machine

The SPI master has been designed for the LTC2314-14 ADC according to the ADC timing requirements. The implemented SPI master activates the chip select, applies the required setup timing, generates the SPI clock sequence, reads the serial ADC data, and asserts a data-ready flag once the conversion word is available. The SPI acquisition module has been tested with a 50 MHz FPGA input clock and a 25 MHz SPI clock. Under this configuration, one SPI transaction takes approximately 1.3 µs, which satisfies the current system requirements.

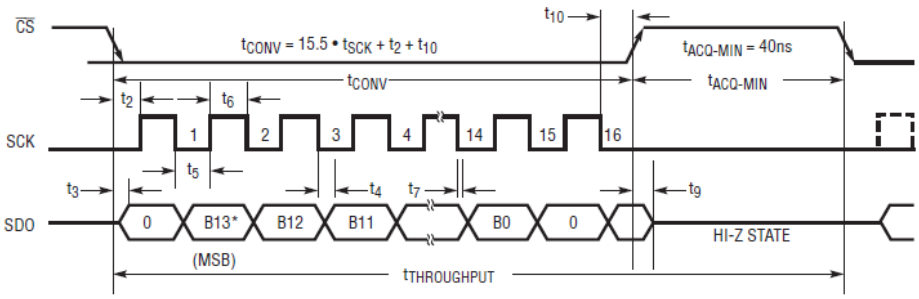


Figure 2-5: SPI transaction timing diagram

At the current development stage, the SPI master for ADC data acquisition has been implemented in Verilog and tested under the stated clock conditions. However, not all blocks shown in the overall system architecture are fully implemented.

2.1.1.4 High-Bandwidth Sensing and Burst-Mode ADC Specification for Adaptive Smart Gate Driver ICs (UC2b)

An adaptive smart gate driver IC is being developed to enable high-speed closed-loop control of switching transitions in wide-bandgap power semiconductor devices. The approach combines an adaptive digital gate driver with a co-integrated high-speed ADC to measure transient terminal voltages during turn-on and turn-off events. The measured transient terminal voltages are used to extract switching features such as slew rate, voltage overshoot, and ringing behaviour for gate-current profile adjustment.

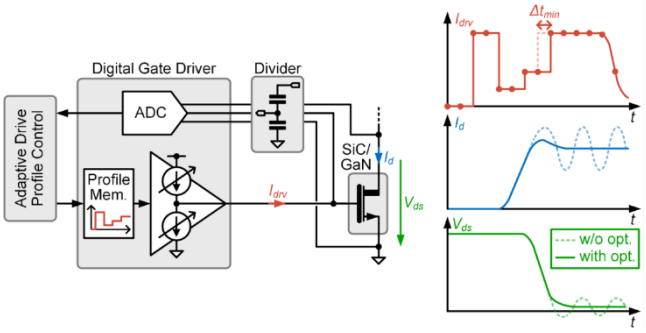


Figure 2-6: System overview of the intelligent adaptive gate driver IC

During the reporting period, the concept planning, technology selection, and transistor-level implementation of the high-bandwidth sensing system integrated in the smart gate driver IC were performed. The requirements and specifications for the target application were defined, and initial transient switching simulations of SiC and GaN devices were carried out using manufacturers' SPICE models. Based on these simulations, the relevant measurement quantities for adaptive switching profile optimization were identified, including voltage and current slew rates, overshoot levels, and ringing frequency.

The sensing concept relies on co-integration of a high-speed ADC on the same silicon die as the gate driver. This integration reduces parasitic effects in the measurement loop and thus enables compact implementation on the converter PCB. The design must address the different operating voltage requirements of SiC and GaN devices, including the higher positive and negative gate-source voltage levels required for SiC MOSFETs and the lower gate-drive voltage range required for GaN devices.

A suitable high-voltage CMOS technology was selected for the implementation. The selected technology is X-Fab XT018, a 180 nm BCD-on-SOI technology offering dielectric high-voltage isolation and multiple high-voltage device options. The selection was based on the need to withstand operating voltages of at least 20 V, while also providing sufficiently fast low-voltage circuitry, acceptable area overhead for high-voltage isolation, and suitable metallization properties for gate-driver output current capability.

To capture the fast-switching transitions of GaN and SiC devices, a burst-mode ADC architecture was defined for the high-bandwidth sensing concept. In this architecture, the ADC operation is divided into a burst phase and a conversion phase. During the burst phase, the power transistor terminal voltage is sampled by an interleaved sampling stage at a sampling rate above 1 GS/s and stored as analog voltages on sampling capacitors. During the conversion phase, the stored samples are converted using a slower shared ADC core. This decouples the high sampling-rate requirement from the overall conversion rate and enables high time-resolution acquisition during the short switching transition window.

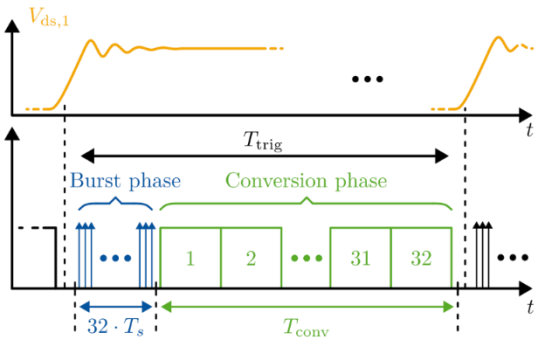


Figure 2-7: Burst-mode ADC operation and conceptual timing diagram

The intended measurement system includes scaling of the drain-source voltage before sampling, since the targeted power transistor voltage is nominally 400 V and may reach up to 650 V during transient events. The burst-mode sampling stage uses parallel track-and-hold channels to capture the scaled waveform during the switching event. The sampled voltages are then multiplexed to a shared ADC core for digitization.

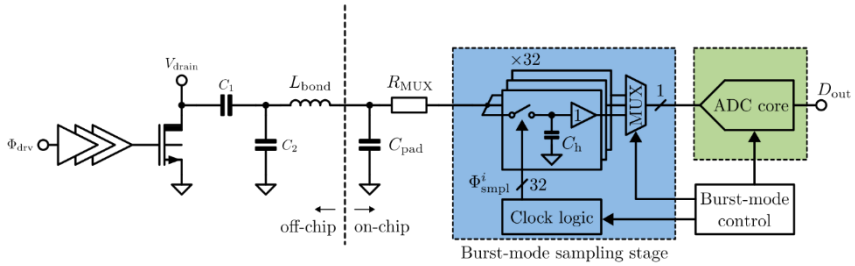


Figure 2-8: Power transistor with drain voltage divider and conceptual on-chip burst-mode ADC

Simulation results were used to derive the ADC specifications. The target sampling rate was determined as greater than 2.5 GS/s, in order to match the required time resolution of the gate driver and provide sufficient information for closed-loop switching optimization. A configuration with 32 parallel track-and-hold channels was selected, resulting in an observable time window of 12.8 ns at 2.5 GS/s. To increase flexibility, the burst stage is designed to include a configurable sampling rate and a programmable delay between the gate-driver operation and ADC sampling. This allows the sampling window to be shifted to the relevant part of the switching waveform and enables repeated measurements over consecutive switching cycles under periodic steady-state operation.

The simulations also indicated that high-frequency ringing in the range of several hundred MHz can occur during switching transitions. Therefore, an ADC bandwidth above 300 MHz was specified. A target resolution of 8 bit was determined to be sufficient for extracting the relevant waveform parameters required for adaptive switching profile optimization.

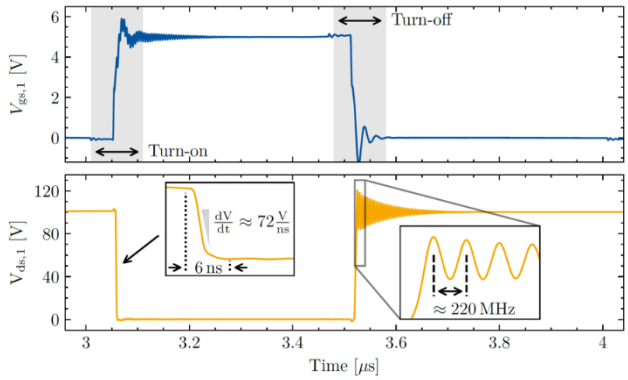


Figure 2-9: Simulated waveforms of a fast-switching GaN device

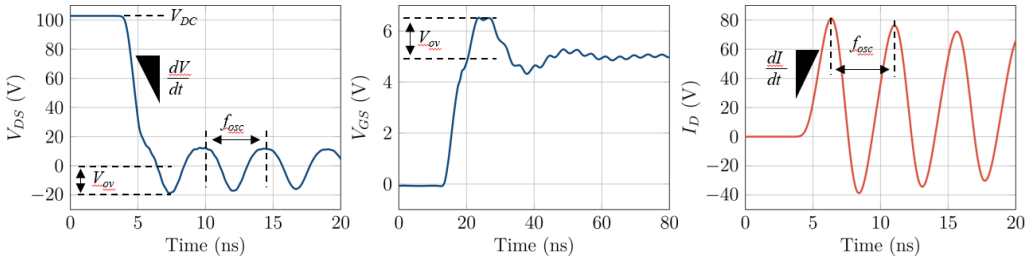


Figure 2-10: Investigation of the relevant quantities for the switching profile optimization

2.1.2 Advanced Control for High Switching Frequency WBG-Based Converters

This section covers developed control techniques for high-switching-frequency WBG-based converters at the simulation level. First, adaptive gate-driver control for optimizing power-device switching profiles is described. Next, PWM generation strategies and DC-link voltage balancing are assessed by simulation. Then, a control optimization study for high-frequency DC-DC converters is presented. In addition, an advanced control strategy for high-efficiency operation of a DC-DC converter is introduced. Finally, a control concept for regenerative braking under battery charging limitations concludes this section.

2.1.2.1 Adaptive Gate-Driver Control for WBG Switching-Profile Optimization (UC2b)

The adaptive digital gate driver IC architecture defines a flexible platform for cycle-by-cycle optimization of switching transitions in wide-bandgap power transistors. The system combines a programmable gate driver ASIC, an integrated ADC interface, SPI-based register access, and an external control environment for adaptive switching-profile optimization.

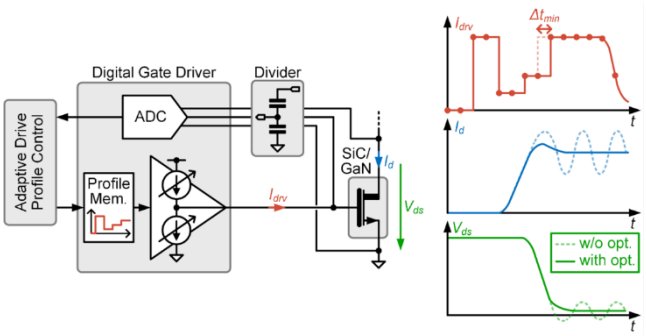


Figure 2-11: System overview of the intelligent adaptive gate driver IC

The architecture separates the adaptive control algorithm from the gate driver ASIC. Instead of embedding the control strategy directly into the ASIC hardware, the control loop is assigned to a laboratory PC, which

makes it possible to test and compare different adaptive control strategies without modifying the ASIC design. The ASIC provides an SPI communication interface for programming the gate-drive profile and reading ADC conversion results. An MCU translates the SPI communication to a USB interface, allowing the laboratory PC to access the on-chip registers of the ASIC. This communication structure forms the basis for a digital cycle-by-cycle feedback loop for switching-profile optimization.

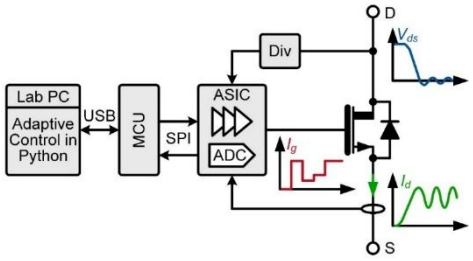


Figure 2-12: System diagram of the communication between gate driver ASIC and lab PC

The demonstrator specification targets operation with wide-bandgap power devices under representative switching conditions. The defined operating range includes a typical DC bus voltage of 400 V, load currents up to 30 A, switching frequencies up to 100 kHz, and drain-source voltage slew rates up to 20 V/ns. The gate driver architecture is specified to support the different gate-voltage requirements of GaN and SiC devices, covering a supply voltage range from 5 V to 20 V and a negative turn-off voltage of typically -5 V for SiC operation.

The demonstrator concept is based on double-pulse testing rather than continuous converter operation. This reduces the complexity of the experimental setup while still enabling characterization of the switching transients and the effect of gate-profile shaping at load currents up to 30 A. The selected device scope includes GaN devices with isolated Schottky-gate structures, GaN gate-injection transistors, and SiC MOSFETs with gate oxide insulation. This device selection allows the gate-driver concept to address different wide-bandgap gate-driving requirements.

The programmable driver stage provides the high timing resolution required for shaping the gate current during fast switching transitions. The 16-phase interleaved clock architecture gives an effective timing resolution of 100 ps for programming the gate-current profile with a finer effective resolution than would be achievable through conventional digital logic timing in the selected 180 nm high-voltage CMOS technology.

The driver stage uses a current-based architecture to support both GaN and SiC gate-drive voltage levels. In this architecture, the output current is defined by programmable current source and sink segments and is largely independent of the selected driver supply voltage. This allows the same driver-stage concept to be applied across the required 5 V to 20 V supply range.

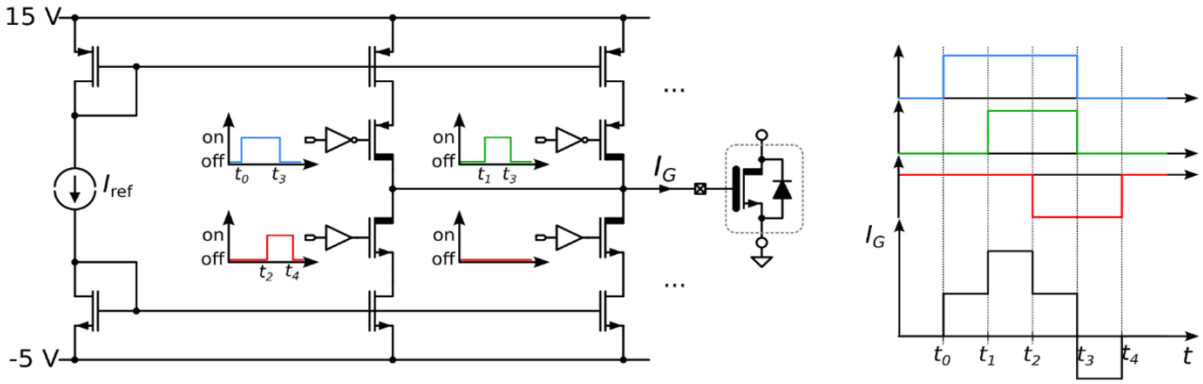


Figure 2-13: Schematic of the current-based driver stage

The transistor-level driver stage consists of parallel PMOS and NMOS current mirror branches whose outputs can be individually enabled through high-voltage switching transistors. The current mirror devices are implemented with 5 V transistors to benefit from improved matching and compact layout, while the switching transistors use a 32 V blocking-voltage rating to provide margin for SiC gate-drive operation. High-speed level shifters provide the required drive signals for the high-side PMOS switching devices.

The resulting driver stage contains 38 parallel NMOS/PMOS current source and sink segment pairs. Thirty-four segments provide 128 mA each, while four smaller segments provide 32 mA each. This gives a maximum programmable source/sink current of approximately 4.5 A with a current resolution of 32 mA. Switching simulations using SPICE transistor models indicate that this current range and resolution are sufficient for precise switching-profile shaping.

2.1.2.2 Simulation-Based Assessment of PWM Generation and DC-Link Voltage Balancing for a T-Type Inverter (UC2b)

The control concept for the high-switching-frequency WBG-based converter includes the selection of a suitable PWM generation strategy and the assessment of DC-link voltage balancing requirements for the T-Type inverter topology. The modulation strategy directly affects waveform quality, neutral-point behaviour, and switching-related losses.

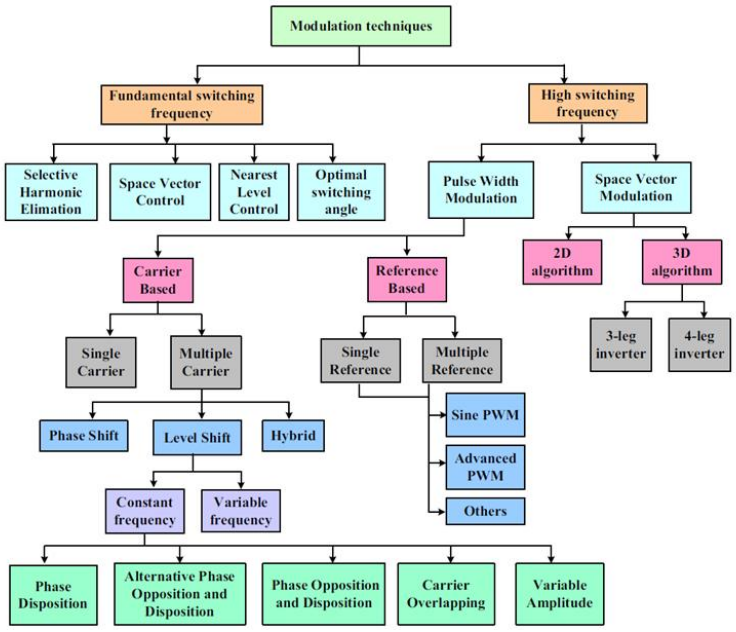
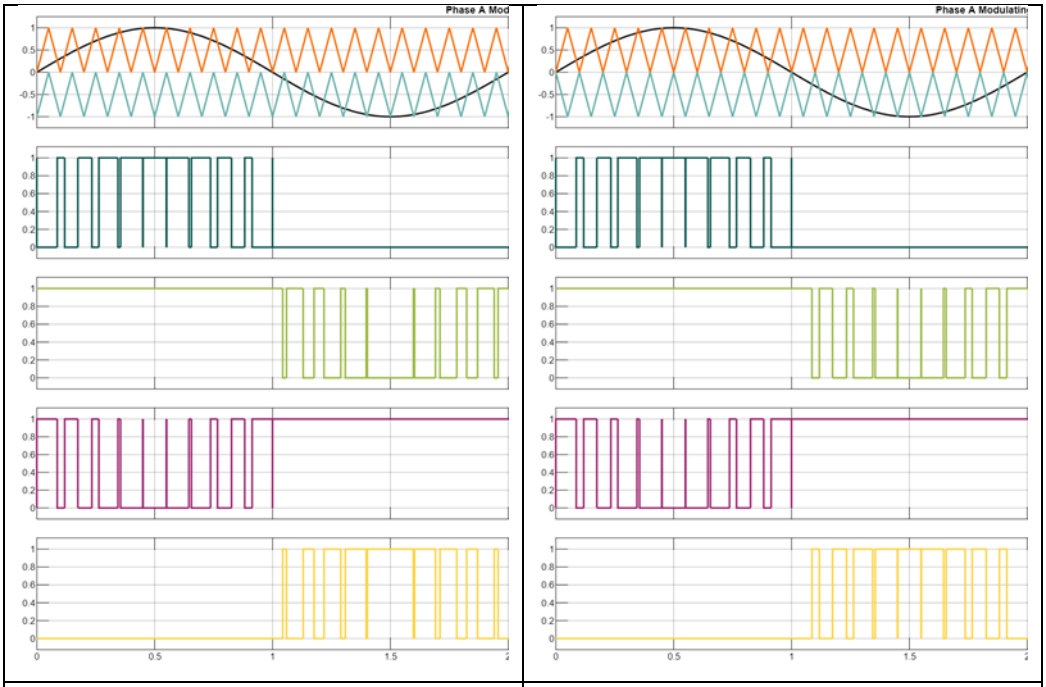


Figure 2-14: Modulation Techniques Flowchart

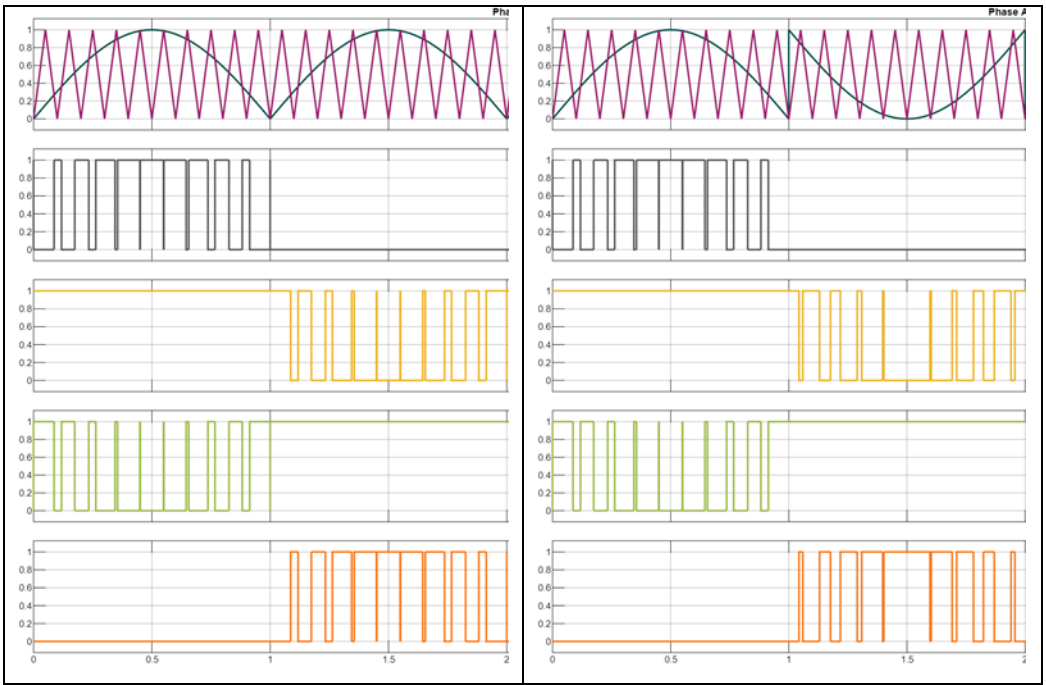
For the considered use case, PWM is used to generate the switching-state pulses. In a conventional three-level PWM implementation, two carrier signals and one reference signal per phase are typically required to generate the switching signals for each inverter leg. However, the available microcontroller hardware is limited to one carrier signal. Therefore, two implementation approaches have been identified: using two reference signals with one carrier signal or using a modified reference signal with a single carrier signal.

Different multilevel PWM strategies were reviewed, including multi-carrier PWM approaches such as phase-shifted and level-shifted PWM, as well as single-carrier PWM approaches. Level-shifted PWM variants, including in-phase disposition, phase opposition disposition, and alternate phase opposition disposition, were considered because of their relevance for multilevel inverter operation and harmonic performance. Single-carrier PWM approaches were also considered as implementation alternatives under the given hardware constraints.



In-Phase Disposition (IPD) PWM	Phase Opposition Disposition (POD) PWM

Figure 2-15: Level-shifted PWM



Multi-Modulation Single Carrier PWM	Modified Multi-Modulation Single Carrier PWM

Figure 2-16: Single-carrier PWM

In addition to pulse generation, the DC-link voltage balancing behaviour of the T-Type topology was investigated. The topology can operate either in three-level mode, where the horizontal neutral-point leg

participates in commutation, or in two-level mode, where the converter operates similarly to a B6 bridge. In three-level operation, the neutral point enables the phase voltage levels $+V_{DC}/2$, 0, and $-V_{DC}/2$, but it also introduces the risk of voltage imbalance between the two DC-link capacitors.

A simulation test bench was configured to study the DC-link midpoint imbalance. The analysis was performed for both two-level and three-level operation, with and without a passive balancing bridge. The simulations were carried out using an 800 V DC-link, while the final application is intended for a 400 V DC-link. The input states that the balancing concept remains the same despite the different voltage level.

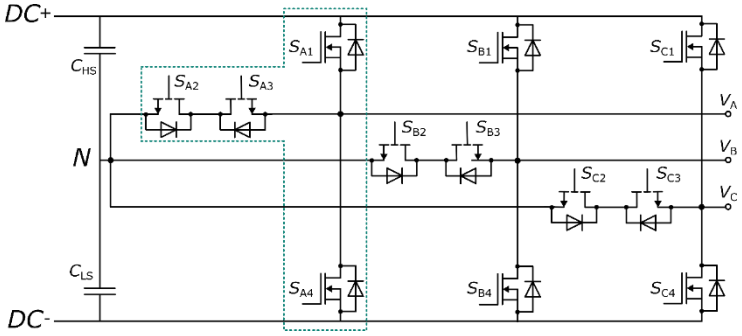
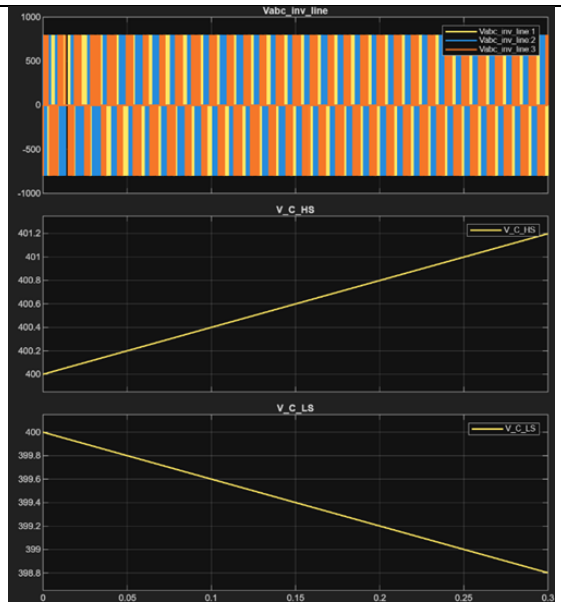
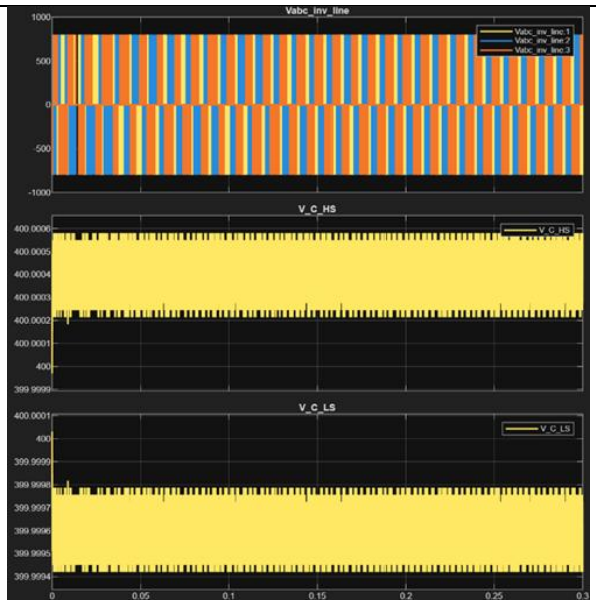


Figure 2-17: Switching State representation for T-Type Topology

In two-level operation, the neutral-point switches remain blocked, and the motor load current does not directly influence the midpoint voltage. The observed imbalance is mainly associated with asymmetric high-ohmic measurement paths connected to the DC-link capacitors. Introducing a passive balancing bridge provides a dominant symmetric current path and reduces the resulting capacitor voltage drift. The remaining high-frequency ripple is attributed to PWM switching transients and parasitic coupling rather than a true sustained imbalance.



without balancing network (2-Level operation)

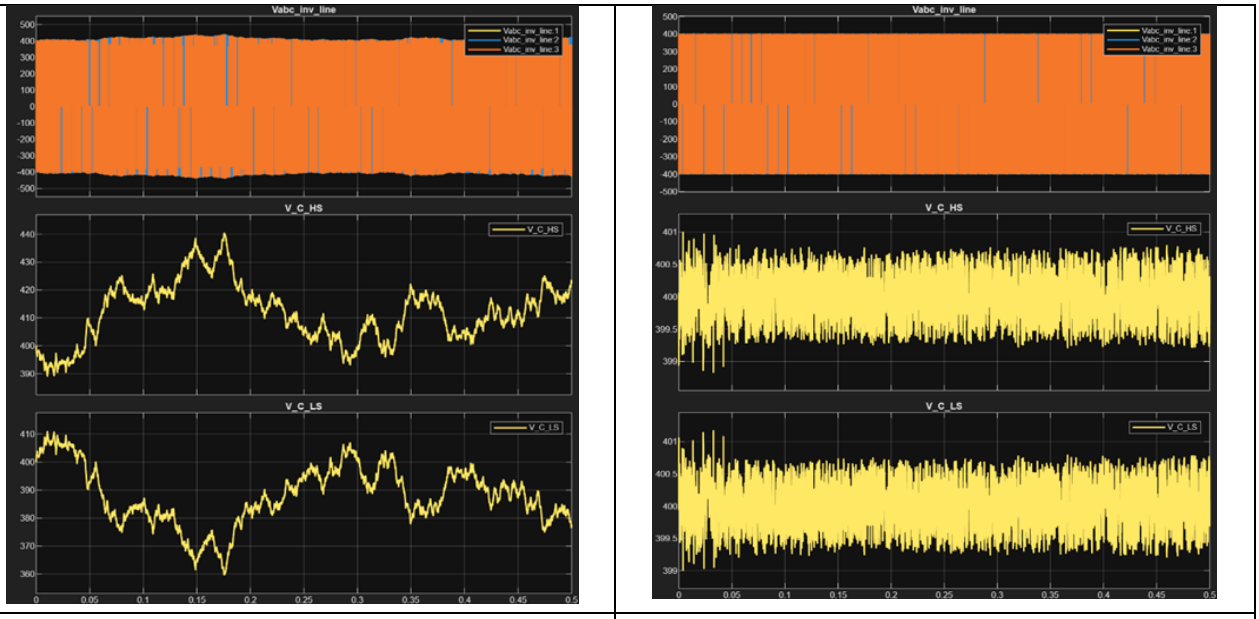


with balancing network (2-Level operation)

Figure 2-18: Charging and Discharging curves of C_{HS} and C_{LS}

In three-level operation, the neutral point is actively connected to the load during the zero-voltage switching state. As a result, load currents flow into and out of the midpoint and directly affect the charge balance of the upper and lower DC-link capacitors. Without a passive balancing bridge, the simulations show large

dynamic capacitor-voltage deviations. With the passive balancing bridge, the voltage excursions are significantly reduced. However, residual oscillations remain because the passive bridge cannot fully compensate the dynamic neutral-point currents occurring during three-level operation.



without balancing network (3-Level operation)	with balancing network (3-Level operation)

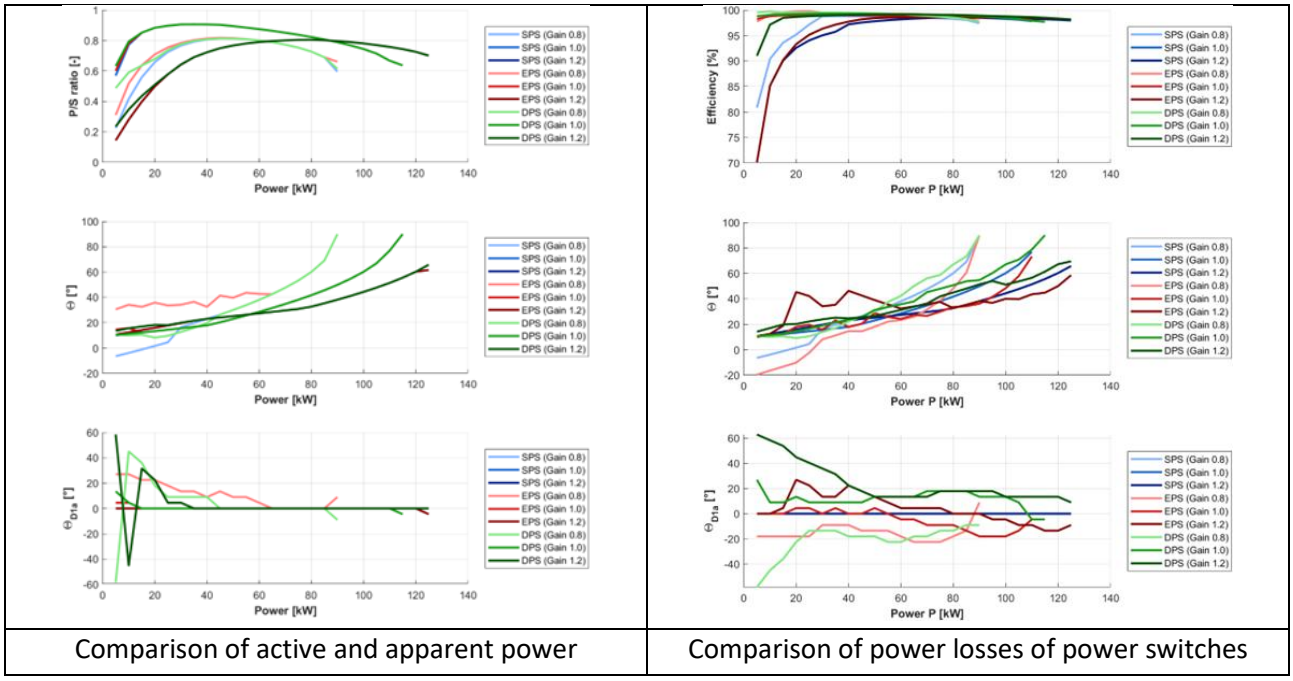
Figure 2-19: Charging and Discharging curves of C_{HS} and C_{LS}

The simulation results indicate that passive balancing can mitigate excessive DC-link voltage excursions, particularly under fixed or simplified operating conditions. However, for dynamic operation over a wide speed and torque range, an active DC-link voltage balancing algorithm is required to dynamically control the neutral-point current and maintain capacitor voltage balance.

2.1.2.3 Control Optimization Study for High-Frequency DC-DC Converters (UC6)

A control optimization study was carried out for a dual active bridge converter with a target power of 125 kW and an output voltage of 1500 V. The study considered both converter parameter design and modulation strategy selection, with a focus on achieving high efficiency and suitable operating characteristics.

The investigated control strategies include single phase shift, enhanced phase shift, and dual phase shift control. For these modulation methods, the phase-shift angle was systematically evaluated under different operating conditions. The analysis considered the relationship between active and apparent power, converter efficiency characteristics, and power losses in the power switches.



Comparison of active and apparent power	Comparison of power losses of power switches

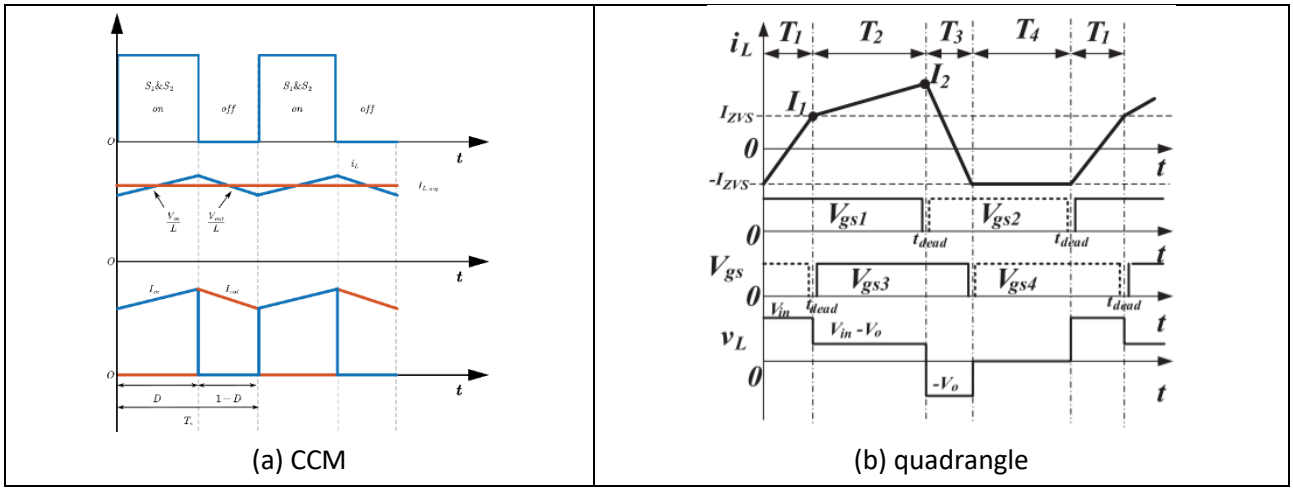
Figure 2-20: Control of DAB converter, targeting to power of 125 kW and output voltage of 1500 V, study of single-phase shift, enhanced phase shift and dual phase shift control

The results illustrate the optimization-oriented study, including the relationships between active and reactive power, converter efficiency characteristics, and the resulting voltage gain behaviour. These findings provide important insights for determining the final optimal transformer turns ratio and for improving the overall performance of the DAB converter system.

2.1.2.4 Advanced Control for High-Efficiency Operation of DC-DC Converter (UC1)

A constant-switching-frequency operating strategy was assessed for the UC1 bidirectional DC-DC converter, with a focus on switching-sequence design, current shaping, and their impact on converter operating characteristics. Following a preliminary screening of candidate converter structures and auxiliary soft-switching concepts, the two-level four-switch buck-boost (2L4SBB) converter was selected as the reference platform for comparing operating modes under identical converter structure and operating conditions.

The assessment compared continuous conduction mode and quadrangle operation under constant switching frequency. Continuous conduction mode was used as the reference case, providing the conventional inductor-current waveform and a baseline for comparison. Quadrangle operation introduces multiple controlled subintervals within one switching period, thereby modifying the inductor-current trajectory and the current levels at the switching instants.



(a) CCM (b) quadrangle

Figure 2-21: Comparison of CCM and quadrangle operation for the 2L4SBB under constant switching frequency

Under constant switching frequency, the switching period remains fixed, while the sequence and duration of the internal subintervals serve as the main control variables. The quadrangle operating mode was therefore assessed as a method to shape the inductor-current waveform and to evaluate whether more favourable switching conditions, including ZVS or partial-ZVS operation, can be approached while maintaining the required power transfer.

A mathematical description of the quadrangle waveform was developed by representing the inductor current as a piecewise-linear function over the switching subintervals. This approach links the timing variables to the current trajectory, transferred power, and current available at the switching instants, while also enabling assessment of soft-switching conditions, feasible operating regions, timing limits, and maximum transferable power. The resulting framework was then applied in a preliminary numerical evaluation under representative operating points. The evaluation considered 15 kW module operation, operating points of 400 V / 900 V and 800 V / 900 V, and both power-flow directions. The numerical analysis was used to compare the current trajectories and operating feasibility of continuous conduction mode and quadrangle operation.

The preliminary comparison shows a clear trade-off between magnetic energy requirements and current stress. For the evaluated operating point, quadrangle operation reduces the required inductance from 49 µH to 9.9 µH and the stored magnetic energy from 0.05 J to 0.03 J. However, this is accompanied by an increase in peak inductor current from 45A to 77.86 A and RMS inductor current from 37.749 A to 45.49 A.

Parameter	CCM	Quadrangle
Peak inductor current, $\hat{I}_L$(A)	45.00	77.86
RMS inductor current, $I_{L,\mathrm{RMS}}$(A)	37.749	45.49
Inductance, $L(\mu\mathrm{H})$	49.0	9.9
Stored magnetic energy, E(J)	0.05	0.03

Table 2-1: Preliminary operating-point comparison of CCM and quadrangle operation for the 2L4SBB

These results show that quadrangle operation substantially changes the internal current trajectory compared with continuous conduction mode. The reduced inductance requirement indicates a potential benefit for the converter magnetic design, while the increased peak and RMS current indicate higher current stress and potentially higher conduction losses. Therefore, the benefit of quadrangle operation cannot be assessed solely based on improved switching conditions; the current-stress penalty must also be considered.

The assessment identifies quadrangle operation as a relevant advanced operating mode for further development, but not as a finalized operating strategy. The main remaining control challenge is the determination of a quadrangle timing pattern that maintains favourable switching conditions while reducing the peak- and RMS-current penalty. Preliminary efficiency estimates for the selected two-level four-switch buck-boost converter are in the range of 98–99%; however, the operating region in which quadrangle operation contributes most effectively to this target remains under evaluation.

2.1.2.5 Advanced Control for Regenerative Braking under Battery Charging Limitations (UC4b)

Regenerative braking in electric vehicles normally aims to recover kinetic energy and return it to the battery. Under nominal operating conditions, the electric machine operates as a generator during braking, and the recovered energy is transferred through the inverter to the DC link and subsequently to the battery. This process allows part of the braking energy to be recovered instead of being dissipated mechanically or thermally, provided that the battery can accept the charging power.

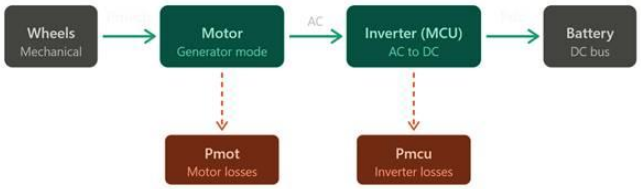


Figure 2-22: Energy-flow diagram during regenerative braking

During regenerative braking, mechanical power from the wheels is converted by the electric machine, which operates as a generator. The generated AC power is processed by the inverter and converted into DC power intended for the battery. Along this path, losses occur in both the motor and the inverter. Motor losses are mainly dissipated as heat in the windings, while inverter losses are dissipated in the power electronics.

However, regenerative braking capability can be limited when the battery cannot accept the generated charging power. This can occur under conditions such as low battery temperature, elevated battery temperature, or high state of charge. In such cases, the permissible charging current may be significantly reduced, potentially down to zero. If no alternative energy path is available, the available regenerative braking torque is reduced accordingly, which may lead to an inconsistent braking response from the driver's perspective.

The Out-of-Phase concept addresses battery-limited regenerative braking by providing an additional braking-torque contribution without requiring the corresponding electrical power to be absorbed by the battery. Instead, the unwanted energy is intentionally dissipated as heat in the motor windings. In this operating mode, the motor acts not only as a generator but also as a controllable electrical load, which can generate braking torque even when the battery charging-power limit is reduced.

The control concept is based on the calculation of four torque limits in parallel, including the traction limit, the conventional regenerative braking limit, the estimated motor torque, and the extended regenerative braking limit. The extended limit defines the additional braking torque that can be made available if needed. After determining the source of the extra braking torque, the algorithm produces it by intentionally driving extra current through the motor windings such that additional losses are produced in the motor windings.

The vehicle control unit (VCU) activates the Out-of-Phase function only when the requested braking torque exceeds the conventional regenerative braking capability imposed by the battery charging limit. If the requested braking torque remains below the normal regeneration limit, the function remains inactive and the vehicle operates with conventional regenerative braking.

In this approach, the additional braking torque is achieved through intentionally increased motor losses, the motor temperature rises. The concept therefore requires sufficient thermal capacity and cooling capability in the motor.

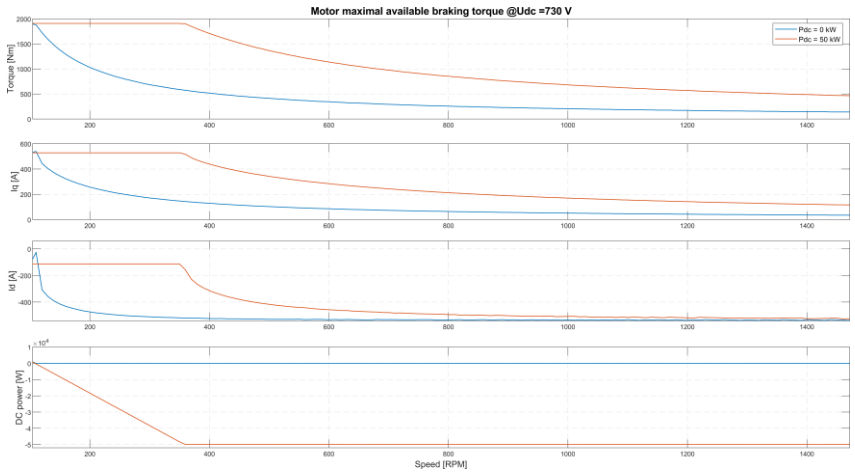


Figure 2-23: Simulation results for maximum Out-of-Phase braking torque at 730 V DC-link voltage

The simulation results show the maximum available Out-of-Phase braking torque. The upper plot shows the maximum available Out-of-Phase braking torque. It can be seen that even at P_{DC}=0 kW, where no power is transferred to the battery, the motor can still provide braking torque at low speeds. This indicates that the concept can maintain braking capability even under highly restrictive battery conditions.

The second plot shows the torque-producing current component, I_q. The current remains close to its rated maximum value over a wide speed range, indicating that the control strategy maintains the current required to generate braking torque.

The third plot shows the direct-axis current component, I_d. The negative values indicate field-weakening operation, which is used to shape the motor operating point and maintain controllability as speed increases.

The lower plot shows the DC power transferred to the battery. The curves remain within the imposed 0 kW and 50 kW limits while additional braking torque is generated through controlled motor-loss production.

2.2 Computational Control for Reliability

This section covers the simulation-based developments carried out within Task 5.2 of Work Package 5. It includes two Subtasks: 5.2.1, which focuses on digital twins for virtual sensing and real-time identification of degradation and design weak points, and 5.2.2, which focuses on AI-enhanced converter thermal control, data-driven cooling unit control, and coordinated control.

2.2.1 Digital Twins for Virtual Sensing & Real-Time Identification of Degradation, Design Weak Points

This section covers activities focused on establishing methodologies and a framework for digital twins, virtual sensing, and real-time identification of degradation in power electronic systems. First, it describes a signal-injection-based degradation diagnosis for converter-fed EESM systems. Next, it presents an embedded thermal sensing method for smart thermal management. Then, it introduces a simulation-based data-generation and digital-twin framework for SoH estimation. Finally, it presents a conceptual framework for building and executing a digital twin.

2.2.1.1 Modulation-Based Thermal Impedance Spectroscopy for Condition Monitoring (UC4a)

A software-based method for targeted thermal excitation via loss manipulation was investigated and assessed for its suitability for detecting degradation in the thermal path of the power module. The approach

is based on a targeted modification of the space-vector modulation. In this method, the zero-vector times within one switching period are distributed asymmetrically, while the durations of the active voltage vectors remain unchanged. The zero-vector distribution factor is defined as

$$\mu = \frac{T_7}{T_0 + T_7} \tag{2-1}$$

and enables the duty cycle of individual switches to be influenced without substantially changing the resulting voltage space vector or the regular inverter operation.

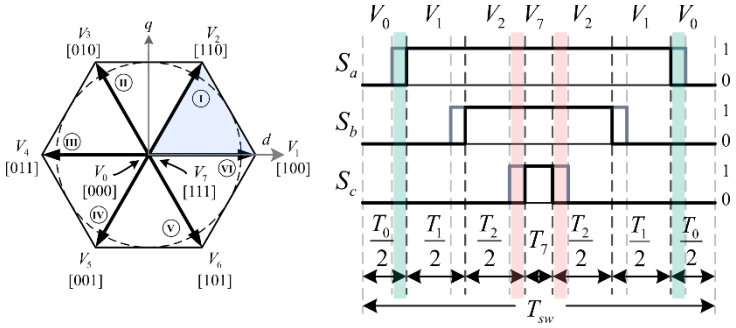


Figure 2-24: Variation of the zero-vector times

A sinusoidal variation of the zero-vector distribution factor generates a periodic change in the duty cycle. Since the conduction losses of a MOSFET are approximately proportional to the duty cycle, this modulation results in a defined sinusoidal loss excitation in the semiconductor. The method, therefore, enables targeted thermal excitation without additional hardware and can, in principle, be applied during inverter operation. A prerequisite is that sufficient zero-vector time is available within the switching period to vary the zero-vector distribution.

To evaluate the method, a simulation workflow was established to analyze the influence of zero-vector variation on the power loss and the resulting junction temperature. The modulation signals, resulting duty cycles, and thermal semiconductor response were analyzed. The evaluation is performed frequency-selectively by determining the relevant signal components at the excitation frequency using an FFT.

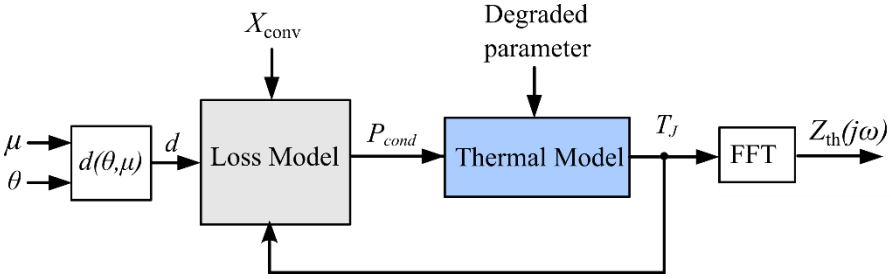


Figure 2-25: Simulation workflow for evaluating loss-based thermal excitation

The simulation results show that a defined periodic loss excitation can be generated by targeted variation of the zero-vector distribution factor. The phase shift between the excited duty cycle or loss excitation and the resulting junction temperature can be used to derive phase information for the thermal transfer behavior.

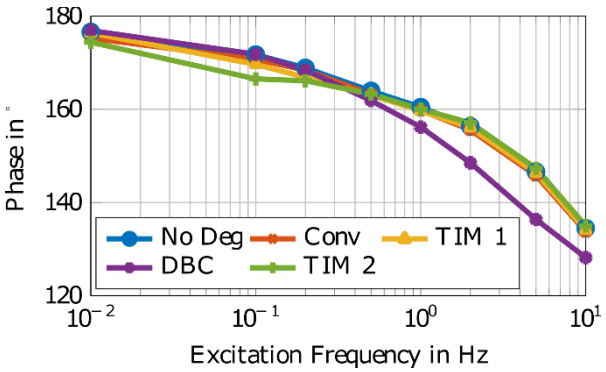


Figure 2-26: Simulation results of the loss-based thermal excitation

2.2.1.2 Signal-Injection-Based Degradation Diagnosis for Converter-Fed EESM Systems (UC4a)

A diagnostic modelling framework was established for the simulation-based detection of progressive winding degradation in electrically excited synchronous machines (EESMs), with a specific focus on inter-turn short circuits (ITSCs). Since winding degradation disturbs the electrical symmetry of the machine, the previously established rotor-oriented (dq)-model was extended to a stator-oriented multi-phase representation in natural coordinates. This phase-domain formulation enables local impedance changes in individual windings to be represented and allows their effects on phase quantities to be analysed.

The adapted EESM model was implemented and compared against the original reference model under fault-free operating conditions. This confirmed consistency with the reference model for healthy operation and provides the modelling basis for subsequent degradation studies. The validation described in the input is therefore limited to fault-free model consistency and does not yet imply experimental validation of the degradation diagnosis.

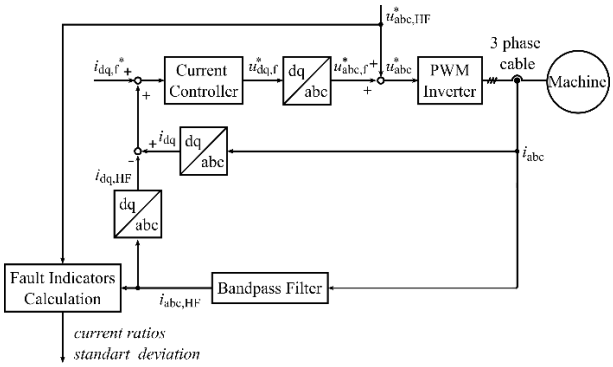


Figure 2-27: Structure or schematic of the stator-oriented multi-phase EESM model for ITSC simulation

A literature-based assessment of signal-injection methods showed that these approaches are well established for other machine types, such as PMSMs [Briz, 2023][Hu, 2021], while their use for EESM winding degradation detection is less established. Existing EESM-related work mainly applies signal injection for sensorless control [Choi, 2013] or thermal monitoring [Laborda, 2025], rather than for the specific detection of winding degradation.

Different voltage-excitation approaches were compared for their suitability for degradation diagnosis. Space-vector-based approaches, including six-step injection and alpha-beta rotating injection, were identified as suitable for detecting faults independently of their spatial position within the phase windings. In contrast, purely axis-based pulsating injection was found to be less suitable for this purpose. Based on its compatibility with existing control structures, the six-step injection method was selected as the basis for further diagnostic investigation. The six-step injection method was assessed through simulation using a validated existing

machine model. The diagnostic evaluation focused on current-based high-frequency response signals. The standard deviation (SD) of the high-frequency current response ratios was used as the diagnostic indicator for winding degradation. The simulation results show a monotonic increase of this indicator with the percentage of shorted turns, indicating sensitivity to progressive ITSC degradation.

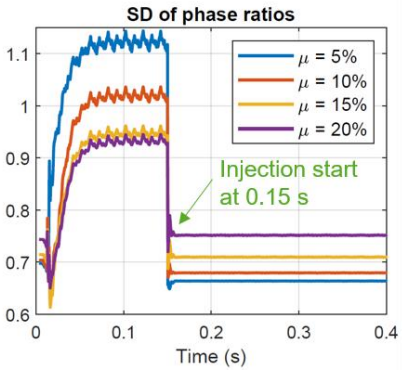


Figure 2-28: Standard deviation of the high-frequency current response ratio

The simulation results indicate high sensitivity in the early degradation range. The low absolute signal level in this range is addressed through synchronous decomposition of the measured response signals. For advanced degradation levels, the indicator reaches a stable saturation range, which can be used for detecting severe fault conditions.

System-technical requirements for signal processing

The following boundary conditions were identified for the reliable measurement of high-frequency (HF) responses:

- Hardware: to maintain the integrity of the HF signals, the current measurement chains must be implemented without analog low-pass filters (anti-aliasing filters). This prevents distortions in both amplitude and phase.
- Software: oversampling of the current signals is required to eliminate aliasing effects during the evaluation of the injected frequency components.

2.2.1.3 Embedded Thermal Sensing for Smart Thermal Management (UC4b)

The smart thermal management of GaN-based power electronics can be achieved by utilizing embedded thermal sensing concepts. The proposed sensor setup combines coolant-temperature measurement and local switch-temperature measurement to provide input data for future virtual temperature-sensing model development.

The sensor arrangement includes two inline temperature sensors located at the inlet and outlet of the cooling plate and one temperature sensor integrated between the cooling plate and the GaN switch. Temperature sensor 1 and 2 are inline temperature sensors with embedded energy harvesting to power the sensor and the communication, while temperature sensor 3 is a thin film printed sensor integrated between the cool plate and the GaN switch. Sensor 3 is a wired and externally powered sensor.

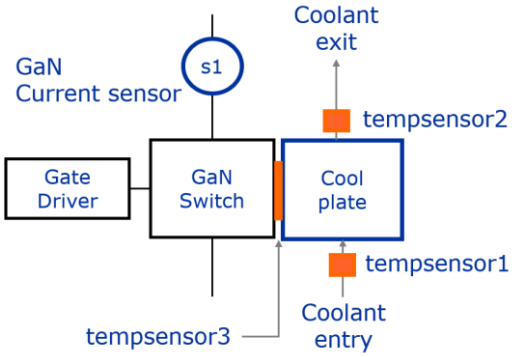


Figure 2-29: Overall sensor setup for GaN switch temperature sensing

The ultra-low-power temperature sensor node is powered by liquid-flow energy harvesting. The concept uses a small magnetic turbine or impeller integrated into the inline housing to harvest hydraulic energy from the coolant flow. The generated electrical output is rectified and stored in a supercapacitor. A low-power microcontroller periodically reads a temperature element, such as an NTC sensor, and transmits the measured temperature using short wireless advertising packets or a low-duty wired digital signal.

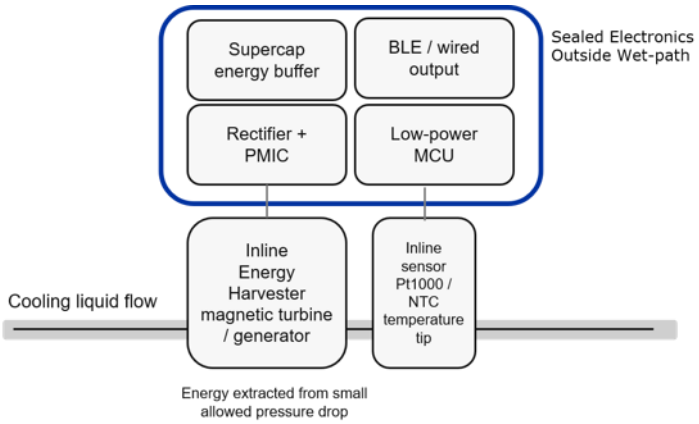


Figure 2-30: Preliminary architecture for inline self-powered temperature sensor

2.2.1.4 Simulation-Based Data Generation and Digital Twin Framework for SoH Estimation (UC2a)

2.2.1.4.1 Simulation-Based Data Generation

A switching-level electrical simulation model was developed in PLECS for the UC2a 3-phase, 3-level hybrid T-type inverter operating from an 800 V DC bus. The simulated inverter topology contains 12 discrete power semiconductor devices and uses a hybrid SiC/GaN device configuration. The topology combines SiC devices in high-stress switching positions with GaN devices in soft-switching positions, with the objective of improving switching performance and efficiency while distributing thermal stress across the semiconductor devices.

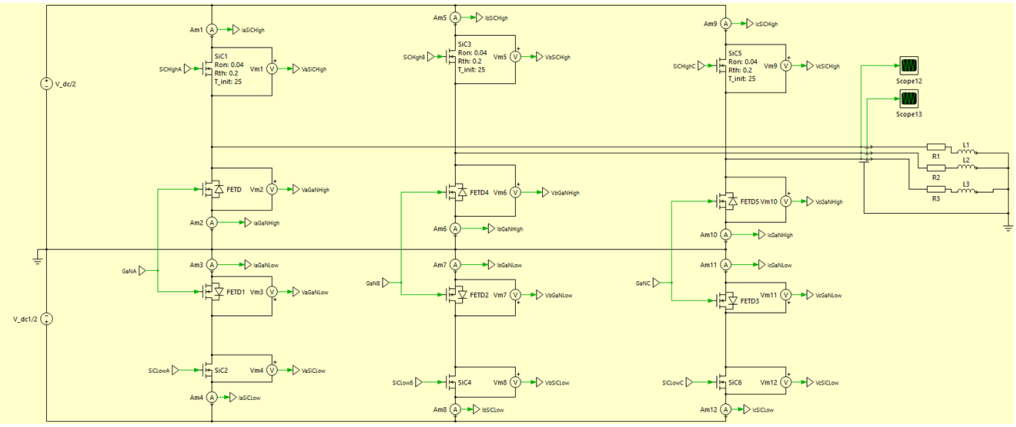


Figure 2-31: Phase 3-Level Hybrid Inverter Electrical Simulation for Data Generation in PLECS

A critical challenge in data-driven prognostics is the scarcity of labelled failure data from aged power devices across their operational lifetime. To address this limitation, a simulation-based data-augmentation strategy is developed that artificially introduces aging effects into electrothermal simulations through degradation models and virtual sensors. Two primary degradation mechanisms are modelled to capture the dominant failure modes in power semiconductor modules:

a. On-Resistance Degradation Model (R_{on}): This model captures progressive on-state resistance increase due to two physical mechanisms: gate oxide trap accumulation, and bond wire degradation due to thermomechanical fatigue
b. Thermal Resistance Degradation Model (R_{th}): This model captures thermal interface degradation primarily due to solder delamination.

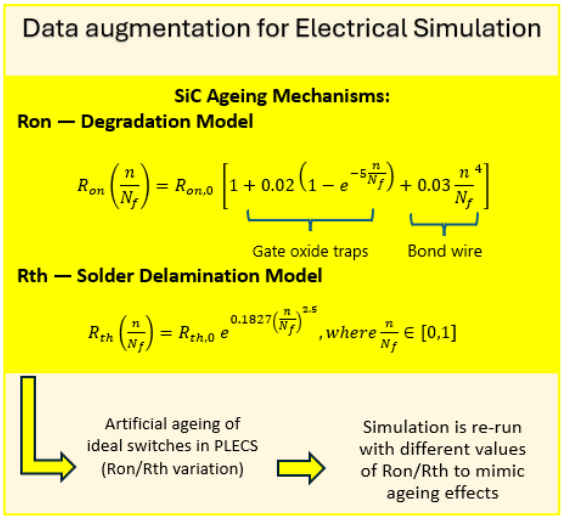


Figure 2-32: Data Augmentation For Electrical Simulation

In the degradation and augmentation process, ideal switches in the PLECS electrical simulation environment are assigned $R_{DS,on}$ and R_{th} values corresponding to different stages of device lifetime. Simulations are re-run iteratively with systematically varied degradation parameters to generate synthetic datasets from beginning-of-life to end-of-life conditions. This approach enables the generation of extensive labelled training data without requiring physical accelerated aging tests on hundreds of devices. The electrical simulation layer uses PLECS to model the inverter's electrical behaviour at switching-level fidelity. The generated instantaneous-loss data are used as input to the thermal simulation in OpenFOAM. The coupled electrothermal simulation

framework generates comprehensive time-series datasets containing electrical quantities via virtual sensors, including voltage and current, thermal quantities, including junction temperature and ambient temperature, and degradation indicators, including $R_{DS,on}$ and R_{th}, for each of the 12 semiconductor devices under realistic automotive operating conditions.

The simulation-generated data undergo feature extraction to derive health indicators, including forward voltage drop, junction temperature, and thermal resistance. State-of-health labels are derived from physics-based failure criteria. Supervised machine-learning models are trained on the labelled dataset to map features to SoH values for real-time health estimation.

2.2.1.4.2 Thermal Digital Twin

Thermal digital twin framework facilitates real-time thermal prediction. The framework is based on an Operator Inference (OpInf) reduced-order model (ROM) and is structured into three stages: training database generation, offline reduced-order model construction, and online prediction. The training database is generated from high-fidelity thermal simulations.

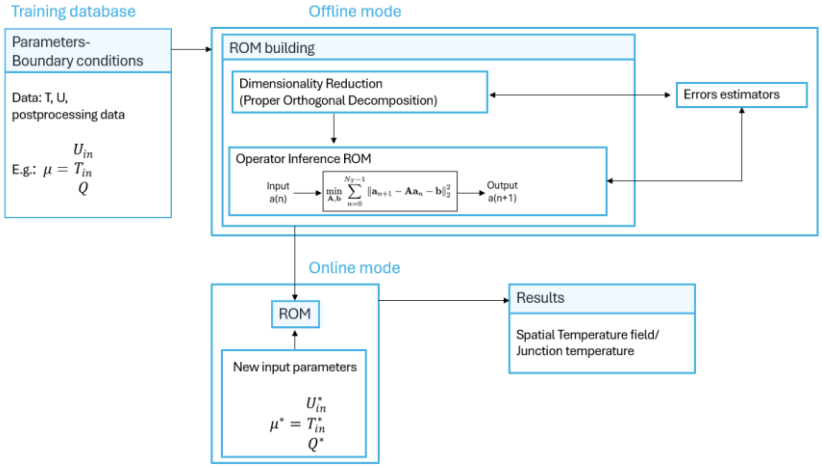


Figure 2-33: Thermal digital twin framework

The offline phase is dedicated to constructing the ROM. First, dimensionality reduction using Proper Orthogonal Decomposition is applied to extract dominant modes from the high-dimensional temperature dataset. This represents the essential thermal dynamics in a low-dimensional subspace while retaining high-dimensional accuracy. An Operator Inference approach is then used to learn the governing reduced-order operators directly from the data. An optimization problem is solved to identify the best-fit operator describing the system evolution. Error estimators are also integrated into the framework to evaluate the accuracy and predictability of the ROM and to support reliability and robustness of the model. In online mode, the built ROM is used to predict the die temperature for unknown parameters, including new inlet mass flow rate, inlet coolant temperature, and heat loss of the SiC/GaN die. The ROM computes the corresponding thermal response without requiring expensive full-order simulation. The online-stage output includes the junction temperature and the full spatial temperature of the die.

2.2.1.5 Development of Framework for Building and Execution of a Digital Twin (UC3b)

In the developed framework, the construction and execution of digital twins are feasible in an accessible and time-efficient manner. The goal is to enable users to create digital twins using predefined building blocks, including users with limited prior expertise. The framework follows the 5D-DT model, which structures the digital twin around five core elements: services, data, physical object, virtual object, and the connections between them. This structure makes it possible to organize the components required for building and executing a digital twin.

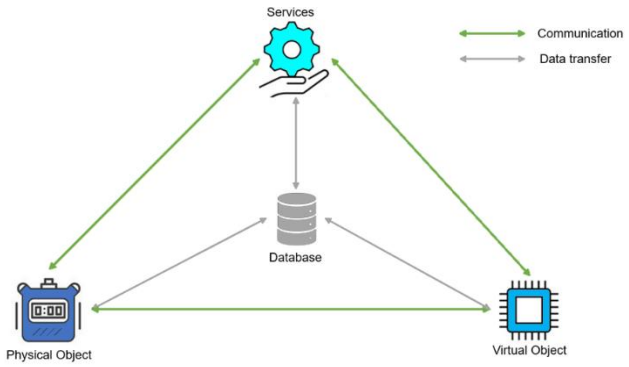


Figure 2-34: Overview of the digital twin framework

A core feature of the framework is its use of Bayesian filters to combine knowledge from physical models with real-time sensor data. By incorporating the uncertainty of both the model and the measured data into the prediction, the resulting output becomes probabilistic. This offers significant advantages in interpreting predictions and in drawing reliable conclusions from them.

2.2.2 AI-Enhanced Converter Thermal Control, Data-Driven Cooling Unit Control and Coordinated Control

This section addresses activities focused on AI-enhanced converter thermal control, data-driven loss reduction, compact digital twin integration, and coordinated control. First, it describes an online adaptive SVM for active thermal control. Next, it presents a data-driven-based optimization of current-setpoint mapping for multiphase drives.

2.2.2.1 Online Adaptive SVM for Active Thermal Control (UC2a)

An online adaptive space vector modulation (oaSVM) approach has been developed for active thermal control (ATC) at the modulation level in UC2a. As the first step, a proof-of-concept version of the algorithm was developed for ATC. The simulation results indicate the capability of this approach to handle thermal swings and thermal cycling in medium-voltage, medium-power converters. Then, the approach has been extended to three-level converters, with a particular focus on incorporating operational and safety constraints, such as admissible switching transitions and thermal limits of semiconductor devices.

The proof-of-concept study explores the application of oaSVM to ATC using thermal and loss models, enabling the evaluation of component junction temperatures within a receding-horizon framework. In this way, the switching operation of the converter can be steered toward trajectories that reduce thermal variance and mitigate thermal swings over time. The following figure presents a preliminary simulation result of oaSVM for ATC in a three-level converter.

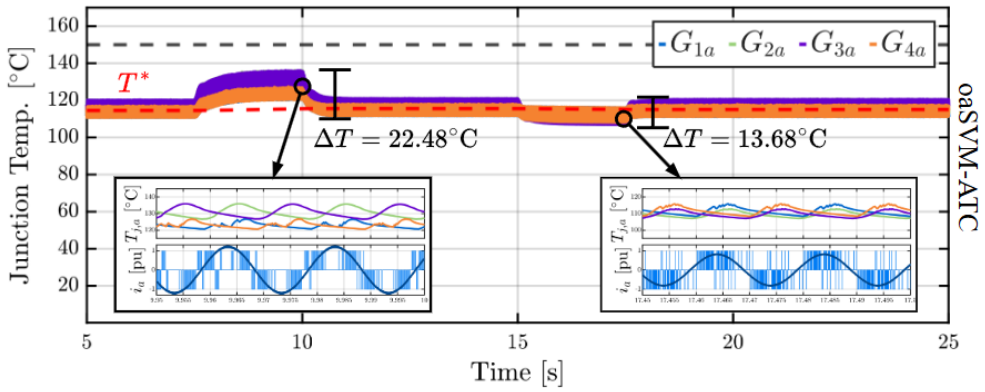


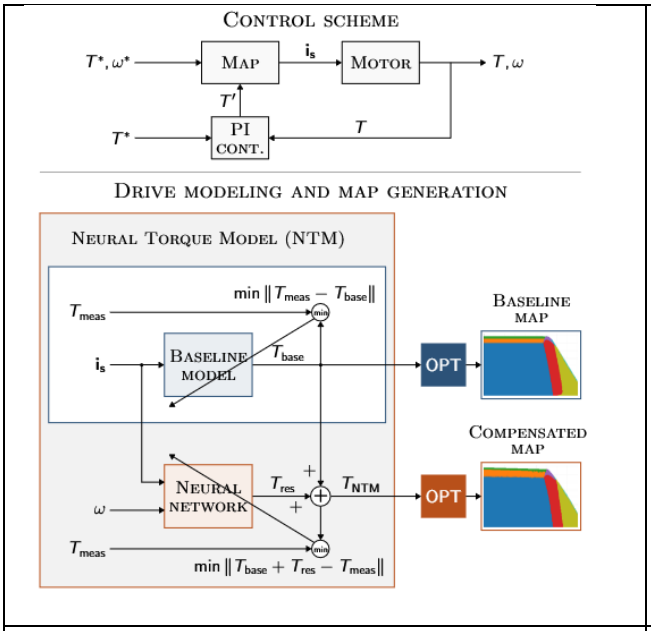
Figure 2-35: Simulation results of oaSVM for ATC under load disturbances: junction temperatures of four switches in the same phase leg, phase a, together with the changes in the switching pattern

A computational complexity analysis shows that a simplified version of the oaSVM algorithm intended for implementation on the Aurix platform, yields an estimated execution time of 0.1 ms.

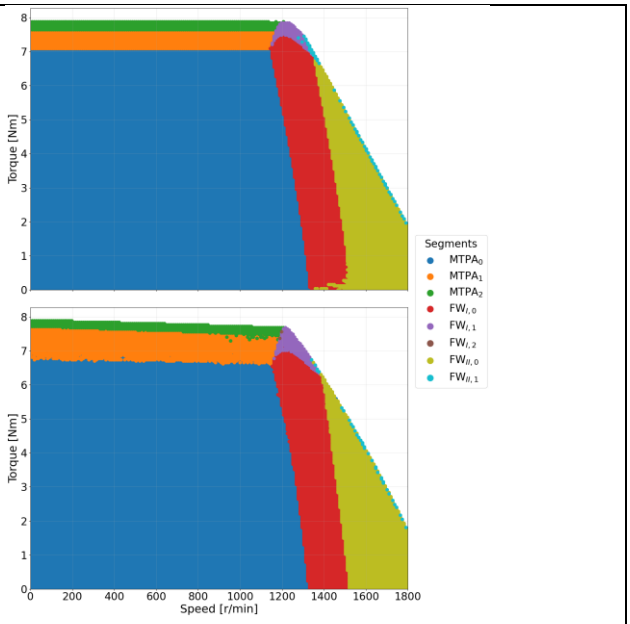
Based on the proposed modulation approach, a coordinated control scheme has been proposed, which is intended to make use of the predictions generated by the PHM digital twin for the real-time tuning of the modulation algorithm, with the aim of reducing thermal stress in semiconductor devices. The key idea is to dynamically adapt the weighting factors of oaSVM without increasing its computational complexity in the base oaSVM version, thus avoiding the need to embed thermal models directly into the controller. The expected benefit is the compensation of transients caused by load variations and changes in the cooling system. For this purpose, the scheme makes use of junction temperature estimations, state-of-health (SoH) information, and the inlet temperature of the cooling system.

2.2.2.2 Data-Driven Optimization of Current-Setpoint Mapping for Multiphase Drives (UC6a)

Higher power density can be realized by multiphase drives, which provide multiple degrees of freedom in current control, allowing additional features such as fault-tolerant operation and torque enhancement through harmonic current injection. These harmonic components offer valuable degrees of freedom for voltage and current waveform optimization, helping to avoid exceeding critical thermal, current, and voltage limits imposed by the converter and motor constraints. Primary optimization efforts focus on minimizing Joule losses and heat production while respecting these operational boundaries. However, initial optimized current setpoints based on analytical models differ from real measured behavior, particularly in high-speed regions where iron losses and other speed-dependent effects become significant contributors to total energy dissipation. To compensate for the difference between analytical models and measured behavior, a neural network-based approach was developed that captures the unmodeled mechanical and iron losses, enabling a more accurate compensated torque-speed map that drives e-drive operation with reduced total losses and controlled heat production.



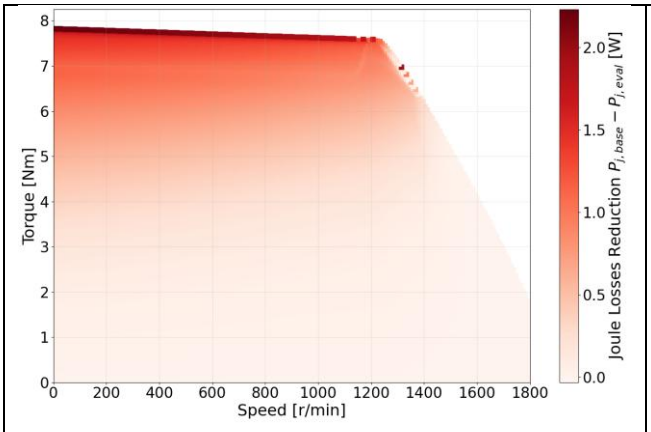
Baseline (top) and the proposed NTM-derived compensated (bottom)



Torque-speed maps with identified operational regions

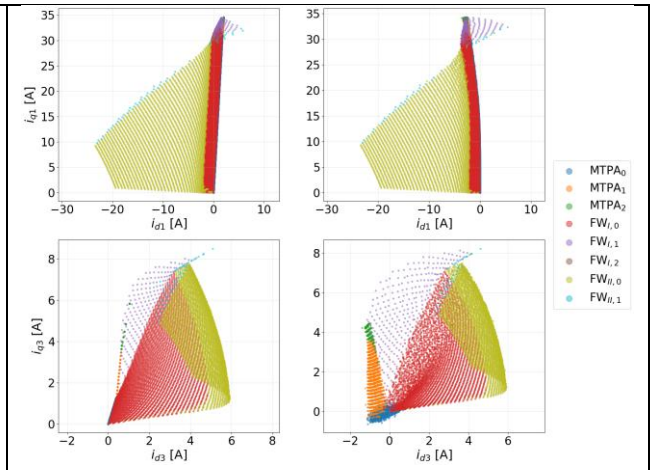
Figure 2-36: Proposed neural torque model for five-phase PMSM drive control to capture unmodeled mechanical and iron losses

By combining a steady-state baseline model with a lightweight neural network, the speed-dependent mechanical and iron losses have been modelled. Compared to the baseline model, the proposed neural torque model (NTM) reduced the torque prediction RMSE and provided a more accurate estimation of the maximum shaft torque. The results of an offline evaluation show that modelling of mechanical and iron losses causes a shift in the optimal operating boundaries of the setpoint maps.



a.

Joule losses reduction between the baseline and the NTM-derived correction map



Optimal current setpoints across operating segments to reduce losses and heat production for the baseline (left) and NTM-derived compensated (right)

Figure 2-37: Joule losses and current trajectory analysis

2.3 Self-Learning Data-Driven Control for Resilience (UC4b)

A machine-learning-based data-driven control architecture has been defined for a wide-bandgap T-Type three-phase three-level inverter driving an in-wheel permanent magnet synchronous motor, as part of UC4b. The concept builds on a baseline Direct Torque Control (DTC), a well-established approach due to its fast dynamic response and inherent field-weakening capability [Takahashi, 1986] and [Depenbrock, 1988], with Space Vector Modulation structure and introduces additional supervisory and optimisation layers to improve adaptability, efficiency, and resilience under varying operating conditions, while incorporating self-learning predictive degradation functions.

2.3.1 Machine-Learning-Based PHM and Derating for Resilience

The proposed architecture combines four main functional elements: the existing DTC-SVM signal processing chain, a Finite Control Set Model Predictive Control (FCS-MPC) [Rodriguez, 2013] core for torque and flux control, a machine-learning-based prognostic health management function with derating capability, and a reinforcement-learning-based speed-controller adaptation layer [Vettor, 2023] adaptation layer. These functions are introduced as enhancements around the baseline control structure rather than as a complete replacement of the drive-control framework.

The target system is an in-wheel traction drive with a 400 V DC bus, an 80 kW-class power rating, and a WBG-based T-Type inverter topology. The switching frequency is treated as an adaptive control output within the MPC-based optimisation. The control concept is intended to support operation over a wide speed and load range, including field-weakening operation and operating conditions affected by component degradation or fault-induced constraints.

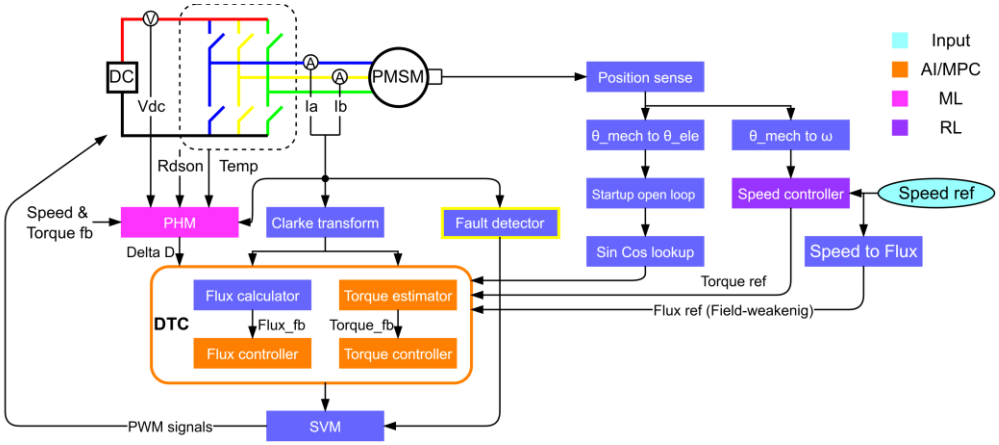


Figure 2-38: DTC-SVM control architecture

2.3.1.1 Existing DTC control

The baseline DTC-SVM path preserves the conventional signal-processing functions required for speed, electrical angle, flux, and torque estimation.

The θ_{mech} to ω block converts the mechanical position to electrical angular speed using the motor pole-pair count. The θ_{mech} to θ_{ele} block produces the electrical angle for the Sin/Cos lookup table and sector identification. Startup open loop control provides a V/f ramp to safely bring the motor from standstill to the minimum speed threshold at which the Torque Estimator and Flux calculator produces a reliable estimate, after which the system transitions to closed-loop control. The Clarke Transform converts the two measured phase currents I_a and I_b into the stationary $\alpha\beta$ reference frame, with the third phase reconstructed via Kirchhoff's current law. The Flux calculator and torque estimator use the $\alpha\beta$ voltage model to compute the stator flux linkage components $\psi_{s\alpha}$ and $\psi_{s\beta}$, the flux magnitude $|\psi_s|$, and the electromagnetic torque T_e. These feedback signals feed directly into the AI/MPC controller.

2.3.1.2 Machine Learning Based PHM Block

The PHM function provides multiple control inputs to the AI/MPC core control algorithm for two primary purposes. The first is to minimize power switch degradation during inverter operation, and the second is to provide derating inputs to satisfy lifetime requirements.

The PHM block is a multi-layer hybrid machine learning based model. The input layers take the data from operational inputs namely, DC link voltage, real speed, torque, coolant temperature, I_a, I_b, and $R_{DS,on}$ sensor data. The health degradation function of the PHM is a pre-trained machine learning model, that gives a rate of damage of GaN power at this current time-step. Mathematically,

$$\Delta D_k = f(x_i), r_k = \frac{\Delta D_k}{T_w} \quad (2\text{-}2)$$

where, ΔD_k is the predicted damage of the switch over a past window of time T_w. The MPC control can use rate of damage r_k to yield a smooth continuous differentiable health degradation indictor trajectory to optimize.

The second block of the PHM is the derating block that will provide a derating indictor $0 < dr < 1$, based on which the AI/MPC core would be able to derate the maximum power output of the inverter to achieve the lifetime goals.

Overall, the PHM function is an intelligent, data-driven system trained using physics-based models and simulation data to achieve its intended functionality. It is also envisioned that the PHM block will be updated through Over-the-Air (OTA) cloud updates to ensure optimal performance throughout the operational lifetime of the system. This capability makes the PHM block a key contributor to resilient and self-learning intelligent control.

2.3.1.3 AI/MPC control core

The Reinforcement Learning (RL) controller supervises the Speed PI controller by continuously adjusting its proportional and integral gains. The RL agent observes the speed tracking error and reward signal and updates the gain schedule without interrupting the control loop.

The Torque & Flux AI/MPC controller replaces the conventional Torque & Flux PI block. It implements a Finite Control Set MPC (FCS-MPC) that enumerates all possible voltage vectors of the T-Type inverter and predicts the resulting torque and flux. The optimal voltage vector is selected by minimising the cost function. The switching frequency becomes an adaptive output of the optimisation rather than a fixed design parameter. The FCS-MPC simultaneously outputs the optimal voltage vector and, critically, sends the optimal Voltage Vectors (VVs) decision to the SVM block which generates PWM for the inverter.

2.3.1.4 Fault Tolerance Integration

The Fault Detector monitors the measured phase currents I_a and I_b. A residual observer compares measured currents with model-predicted values. Open circuit (OC) faults are identified by a phase current collapsing to zero while the reference is non-zero. Short circuit (SC) faults are detected by an over-current condition with a high rate of rise dI/dt. Current sensor faults are identified by a persistent $I_a + I_b + I_c$ offset beyond a threshold. At the hardware level, cycle-by-cycle short-circuit protection on the C2000 will be implemented using the Comparator Subsystem (CMPSS) alongside the ePWM Trip Zone (TZ) mechanism. The trip event simultaneously raises an interrupt, allowing the Fault Detector to classify the fault and decide between derating, shutdown or a restart.

3 Discussion and Conclusions

This preliminary report demonstrates significant progress in the development of advanced control methods for next-generation wide-bandgap (WBG) power electronic systems. The work performed within WP5 establishes a comprehensive foundation that combines high-bandwidth sensing, advanced control algorithms, digital twins, artificial intelligence, and machine-learning-based decision support to improve performance, reliability, and resilience of future electric drive systems. At this stage, the majority of developments have been validated through modelling and simulation activities, providing a solid basis for subsequent hardware implementation and demonstrator validation.

For performance enhancement, the results confirm that high-bandwidth sensing and low-latency measurement architectures are key enablers for exploiting the fast-switching capabilities of SiC and GaN devices. FPGA-based measurement platforms, adaptive gate-driver concepts, and advanced modulation strategies were shown to support more precise switching control, improved converter efficiency, and enhanced protection capabilities. In addition, studies on T-Type inverter modulation, DC-link balancing, and high-frequency DC-DC converter control highlighted the benefits of advanced control approaches while also identifying important design trade-offs between efficiency, switching behaviour, current stress, and implementation complexity.

From a reliability perspective, substantial progress has been achieved in the development of digital-twin-enabled monitoring and control concepts. Novel approaches for thermal impedance spectroscopy, signal-injection-based fault diagnosis, embedded thermal sensing, and simulation-driven state-of-health estimation provide the foundations for real-time condition monitoring and predictive maintenance. The integration of reduced-order thermal models and probabilistic digital twin frameworks enables scalable and computationally efficient virtual sensing solutions capable of supporting operational decision-making throughout the component lifetime.

The work on resilience further extends these capabilities by introducing self-learning control architectures that combine prognostics and health management (PHM), model predictive control, reinforcement learning, and fault-tolerant operation. The proposed concepts demonstrate how future power electronic systems can continuously adapt control parameters according to operating conditions, degradation status, and lifetime objectives. Such adaptive behaviour has the potential to increase system availability, extend useful lifetime, and maintain functionality under adverse operating conditions or partial faults.

Overall, the reported results confirm the strong potential of combining advanced sensing, digital twins, AI-enhanced control, and machine-learning-based health management within a unified control framework. While the current outcomes are primarily simulation-based, they provide clear evidence that data-informed and computationally enhanced control strategies can significantly contribute to higher efficiency, reduced thermal stress, improved fault detection, and increased operational resilience. The next phase of the project will focus on prototype implementation, integration of the developed methods across the HiPower 5.0 demonstrators, and experimental validation under representative operating conditions to quantify the expected benefits and establish technology readiness for future industrial deployment.

4 Terms, Abbreviations and Definitions

HiPower 5.0	Leading edge semiconductor, integration, and control system technologies for highly compact and smart edrive components towards more sustainable power electronics 5.0
2L4SBB	Two-Level Four-Switch Buck-Boost
5D-DT	Five-Dimensional Digital Twin
ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
ATC	Active Thermal Control
CAN	Controller Area Network
DAS	Data Acquisition System
DEC	Websites, patents filing, press & media actions, videos, etc.
DEM	Demonstrator, pilot, prototype, plan designs
DESAT	Desaturation
DMP	Data Management Plan
DSADC	Delta-Sigma ADC
DT	Digital Twin
DTC	Direct Torque Control
EESM	Electrically Excited Synchronous Machine
FCS-MPC	Finite Control Set Model Predictive Control
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
HW	Hardware
IPD	In-Phase Disposition
ITSC	Inter-Turn Short Circuits
NTM	Neural Torque Model
oaSVM	Online Adaptive Space Vector Modulation
OpInf	Operator Inference
OTA	Over-the-Air
PHM	Prognostics and Health Management
PMSM	Permanent Magnet Synchronous Motor
POD	Phase Opposition Disposition
PU	Public, fully open, e.g. web (Deliverables flagged as public will be automatically published in CORDIS project's page)

R	Document, report (excluding the periodic and final reports)
$R_{DS,on}$	On-state resistance
RL	Reinforcement Learning
ROM	Reduced-Order Model
R_{th}	Thermal Resistance
SAR	Successive Approximation
SD	Standard Deviation
SEN	Sensitive, limited under the conditions of the Grant Agreement
SiC	Silicon Carbide
SoC	System-on-Chip
SoH	State of Health
SPI	Serial Peripheral Interface
SVM	Space Vector Modulation
VCU	Vehicle Control Unit
WP	Work Package

Table 4-1: Terms, Abbreviations and Definitions

5 References

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